Reading and writing a disk.

1. In simple applications for disks, most of the times, the data is formatted in fixed record lengths. The disk itself contains sector slots, which enable division of the track into 16 or 24 sectors. By ignoring some of the generated sector pulses it is of course possible to divide a track in 1,2,4,8 and 12 sectors without loosing much storage capacity. This action has to be performed by the control unit.

2. To verify for correct head positioning, each recording cycle has to be preceeded by a reading cycle. When S is the desired sector, then in sector (S-1) the address is read, which normally contains:

   - the head number (0,1)
   - the track number (000-203)
   - the sector number (00 - 16/24)

   When it is checked that the heads are on the correct track, a "full sector" is written after the begin of the next sector mark (pulse).

3. As an example, the sector may contain following information, when using a 16-sector disk and words of 16 bits.

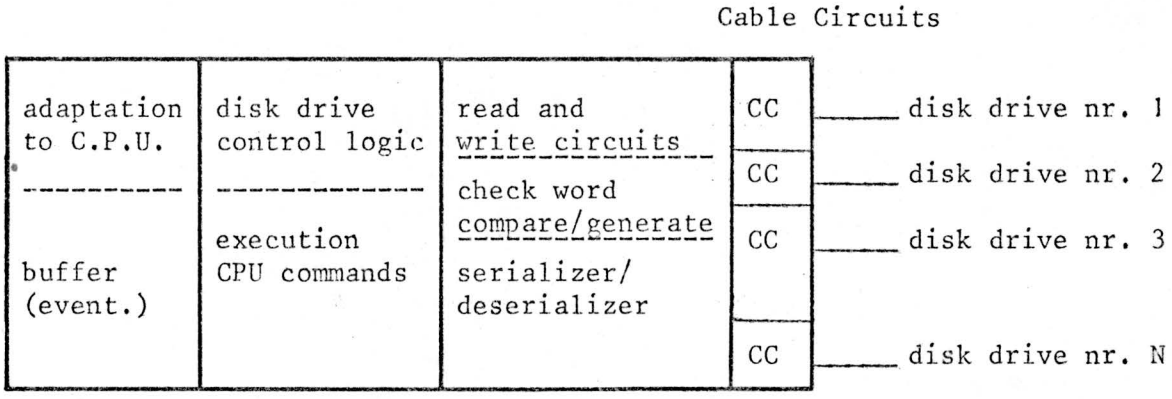
   - pre-amble 14 words
   - synchronisation pattern 1 word
   - data field, including 210 words (maximum)
     sector address, key, data, end of text mark etc.
   - check pattern 1 word
   - post-amble 1 word

4. A write operation starts by switching ON the write and erase enable lines of the disk drive at the leading edge of the sector pulse. At the same time the pre-amble words (bits serialized) are transferred to the drive over the write data line. The simplest way is to write words consisting of all "0"'s. The sync. word may contain fifteen "0"'s and one "1" at the end. A safer way is to use a recognizing pattern like 0000 1110 0000 1110. During a read operation this word should start an operation in the control unit to indicate that next bits are the data field. At the end of the data field, a check word should be written. This word consists of "OR"ed bits of the previous recorded data field words. This is sometimes referred to as sum check or cyclic check.
The post-amble is used to protect the last word against pulse crowding.
The write enable line may be switched OFF now. The erase enable line should remain ON for the duration of 7 words. The reason for this is the physical distance between the gaps of erase heads and write head. The write head records a broad track, which is narrowed by the two erase heads. To be sure that also the last written pattern is narrowed, the erase enable line must be kept ON longer. A write operation should be followed by a read operation, to verify for correct recording.

5. A read operation starts with a delay equal to 5 words from the leading edge of the sector pulse. This is to be sure that reading starts in a well known part of the pre-amble.
The all "0"'s pattern is used to synchronize the read circuits in the disk drive and control unit. The pre-amble, sync. pattern, check pattern and post-amble are normally not transmitted to the C.P.U., but remain inside the Control Unit.

Also these patterns are generated by the Control Unit during a write operation.
During a verify operation (reading after a write operation) a new check word is constructed during the read cycle and this word is compared with the check word stored on the disk during the write operation. When both check words are identical the write operation can be considered as correct.

6. In rough outlines a control unit contains following major four modules.



7. In the enclosed pages, examples of some circuits are described.
Following remarks on the WTR (write) circuit has to be made:

- start is always with a clock pulse after WEN (write enable)
- "keying" a "0" or "1" is by means of SDo.
- SDo is generated by shifting, under control of clock OW
- the write shift register (16 bits) is "emptied" in half words (8 bits); during this phase the new 16 bits are loaded into this register.

During a read operation the action is reversed. The counter shifts the word into the 16 bits register in two parts of 8 bits.

EXAMPLE OF READ/WRITE CIRCUITS.

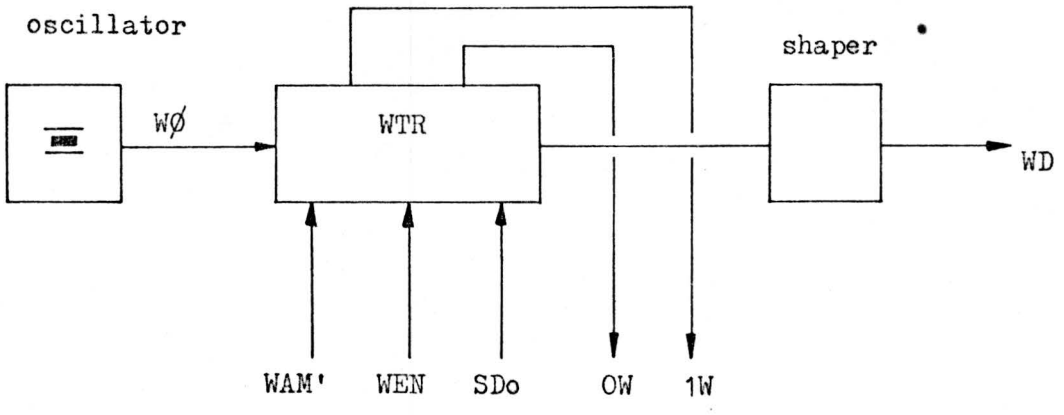
C O N T E N T S P A G E

1. CLOCK-DATA SEPARATOR

1.1. WRITING

The most important parts of the clock-data separator necessary to record data, are:

1. A 1,667 MHz crystal oscillator. → T = 600ns
2. The "WRITE TRIGGER" (WTR), a simulated JK-flip flop which supplies the clock and data pulses (OW, 1W and WD), see page 12 for schematic diagram.
3. A pulseshaper, which forms the pulses for the cable transmitter WD (WRITE DATA) and convert them to the correct width (300 nsec).



Inputs for WTR are:

WØ write oscillator (1,667 MHz square wave
WAM' write address mark (blocking clock pulses)
WEN write enable
SDo Bit o of shiftregister; controls passing of datapulses from oscillator to shaper.

Outputs are:

OW write clock pulse
1W write data pulse
WD write data to mono disk drive

LOGICS OF WTR

WTR 1' : WØ. WTR 2. WTR3. WEN

WTR 2' : WØ. WTR 1. WTR 4. WEN

WTR 3' : WTR 1. WTR 5.

WTR 4' : WTR 2. WTR 6.

WTR 5' : WTR 1. WTR 6

WTR 6' : WTR 2. WTR 5

WD : WEN. WTR 1. WTR 4. SDo. WØ + (data pulse)
WEN. WTR 2. WTR 3. WAM'. WØ (clock pulse)

OW' : WTR 1

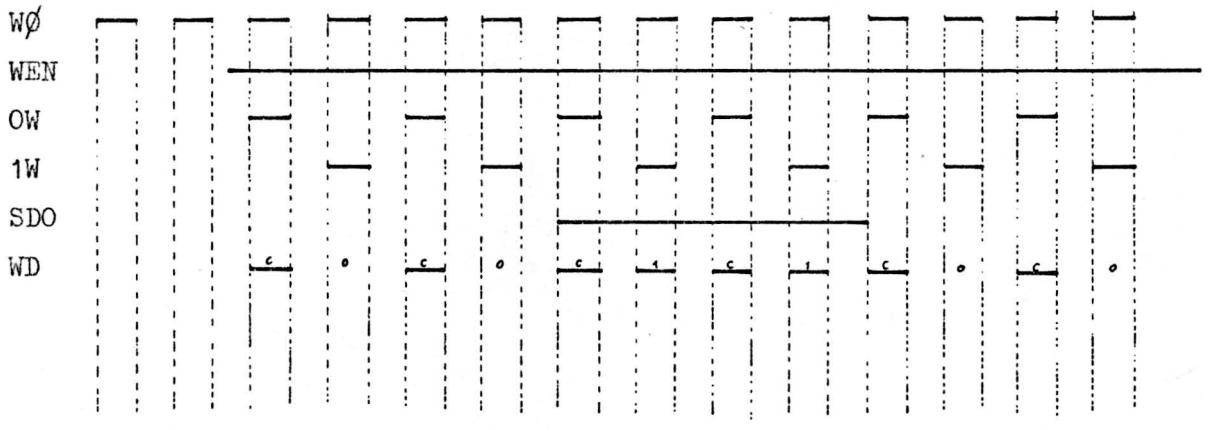
1W' : WTR 2

When WRITE ENABLE (WEN) = true, WTR will count as follows:

WTR	1	2	3	4	5	6	OW	1W
WØ'	1	1	1	0	0	1	0	0
WØ	0	1	1	1	1	0	1	0
WØ'	1	1	0	1	1	0	0	0
WØ	1	0	1	1	0	1	0	1

When WEN=false, WTR stops in position 111001 or 110110;
in these positions OW and 1W are not present.

The signals OW and 1W are used as steppulses in the shiftregister.



During OW , WD depends of WAM (WAM' is always "1")
During 1W , WD depends of SDo (data pulses)

Because of speed considerations the combinations WTR 1. WTR 4 resp. WTR 2. WTR 3 are used instead of 1W and OW as decodings of WD.

1.2 READING

The most important parts of the clock-data separator to read data are:

1. The READ TRIGGER (RTR); same function as WTR during writing, see page 13 for schematic diagram
2. A delay-circuit of 480 nsec.
3. Two pulsshapers for input and output signals
4. The DELAYER TO RESTART (DTR), a RTR-like trigger used at the beginning of reading, see page 14 for schematic diagram.
5. A MISSING PULSE CIRCUIT, used as detector for "0" 's.
6. Some additional logics (START,RTRC,FRDP,etc.)

Inputs of the clock-data separator during reading are:

RED' : READ DATA (incoming data from mono disk drive)

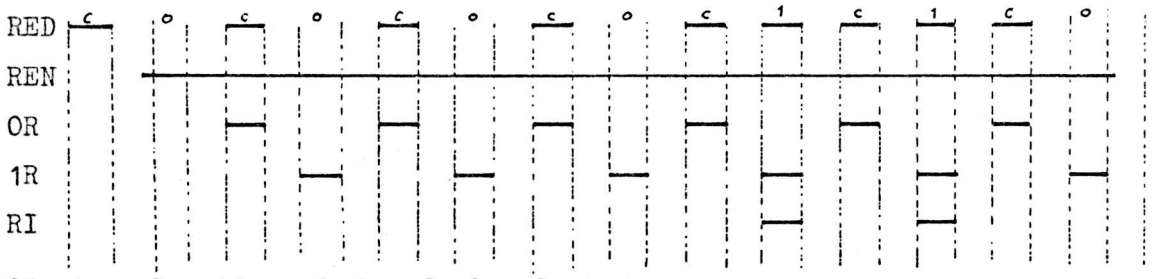
REN : READ ENABLE

Outputs during reading are:

RI : READ INFORMATION

OR : READ CLOCK PULSE

1R : READ DATA PULSE



OR gives location of the clock pulses

1R gives location where ones can be expected

RI gives the actual read ones

RI is sent to the input of the shiftregister; shifting occurs during OR, 1R-pulses.

LOGICS RTR, DTR

RTR'1': RDB. RTR 2. RTR 3. REN +
RD, RTR 2. RTR 3. REN

RTR 2': RDB. RTR 1. RTR 4. REN +
RD. RTR 1. RTR 4. REN

RTR 3': RTR 1. RTR 5

RTR 4': RTR 2. RTR 6

RTR 5': RTR 1. RTR 6

RTR 6': RTR 2. RTR 5. RTRC

RD is READ DATA behind pulseshaper

RDB is the 480 nsec delayed value of RD.

Before beginning reading REN = 0 and RTRC = 0, this causes RTR to stop in position 111001.

At the beginning of reading REN = 1 (RTRC remains a short time = 0), this causes RTR to run in following cycle:

RTR	1	2	3	4	5	6		OR	1R	position
RD'.RDB'	1	1	1	0	0	1	←	0	0	0
RD + RDB	0	1	1	0	1	1	←	1	0	8

OR' : RTR 1

1R' : RTR 2

RI : RTR 1. RTR 4. RD

DTR 1': RD. DTR 2. DTR 3

DTR 2': RD. DTR 1. DTR 4

DTR 3': DTR 1. DTR 5

DTR 4': DTR 2. DTR 6

DTR 5': DTR 1. DTR 6

DTR 6': DTR 2. DTR 5. REN

When REN = 1, DTR will run in following cycle:

DTR	1	2	3	4	5	6	FRDP	position	
RD'	1	1	1	0	0	1	0	0	FRDP=DTR 2'
RD	0	1	1	1	1	0	0	1	(First Read Data Pulse)
RD'	1	1	0	1	1	0	0	2	
RD	1	0	1	1	0	1	1	3	

DTRF 0/DTRF 0' : DTRF 0. REN
DTRF 1. DTR 1'
DTRF 0'

DTRF 1/DTRF 1' : DTRF 1.REN
DTRF 0'. DTR 2'
DTRF 1'

FRDP/FRDP' : DTR 2 +
DTRF 0'
FRDP

START/START' : START. REN
START'. FRDP'

RTRC/RTRC' : RTRC.REN
START.MP
RTRC'

MPI : RD + START'(the Missing Pulse Circuit is triggerd now by RD only when START = 1).

The Missing Pulse circuit supplies an "1" when no new RD-pulse comes within 630 nsec after the trailing edge of an RD-pulse.

The first Missing Pulse starts RTRC = 1, this causes RTR to run as follows:

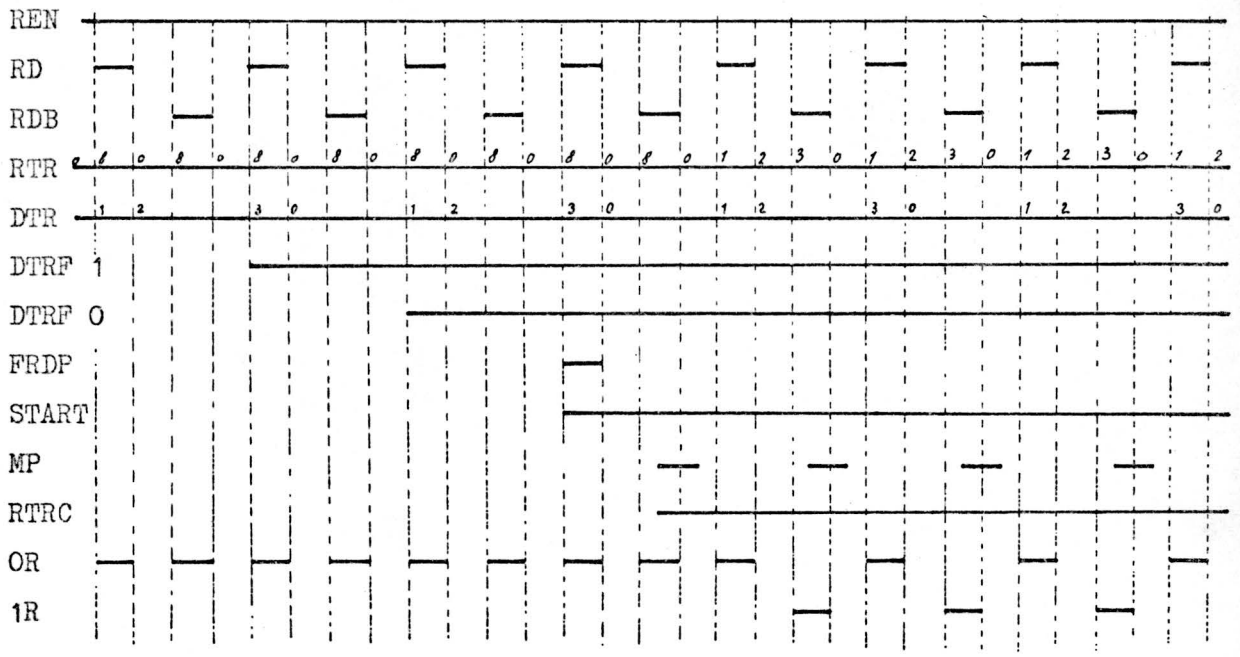
RTR	1	2	3	4	5	6	OR	1R	position
RD'. RDB'	1	1	1	0	0	1	0	0	0
RD + RDB	0	1	1	1	1	0	1	0	1
RD'. RDB'	1	1	0	1	1	0	0	0	2
RD + RDB	1	0	1	1	0	1	0	1	3

The clock-data separator is now synchronised with data coming from the mono disk drive.
All data that is read, will go through the shiftregister; when the synchronizing pattern is recognized (00001110) the Bitcounter and Wordcounter are being synchronized.
Combinations are assembled of the signals OR and OW, resp. 1R and 1W:

ORW = OR + OW
1RW = 1R + 1W

because the shiftregister, bitcounter and wordcounter could be used during reading and writing. Reading and writing never occur at the same time.

1.3 SUMMARY START OF READING



READ ENABLE : = true

The mono disk drive supplies READ DATA, followed by RDB at 480 nsec.

The RTR will go into the cycle 0-8-0-8-etc.

The DTR will go into the cycle 0-1-2-3-0-1-etc.

DTRF 1 will come when DTR is for the first time in position 3, followed by DTRF 0 when DTR is in position 1.

When DTR is in position 3 for the second time, then FRDP will come.

FRDP activates START.

The first "0" after START will set MP.

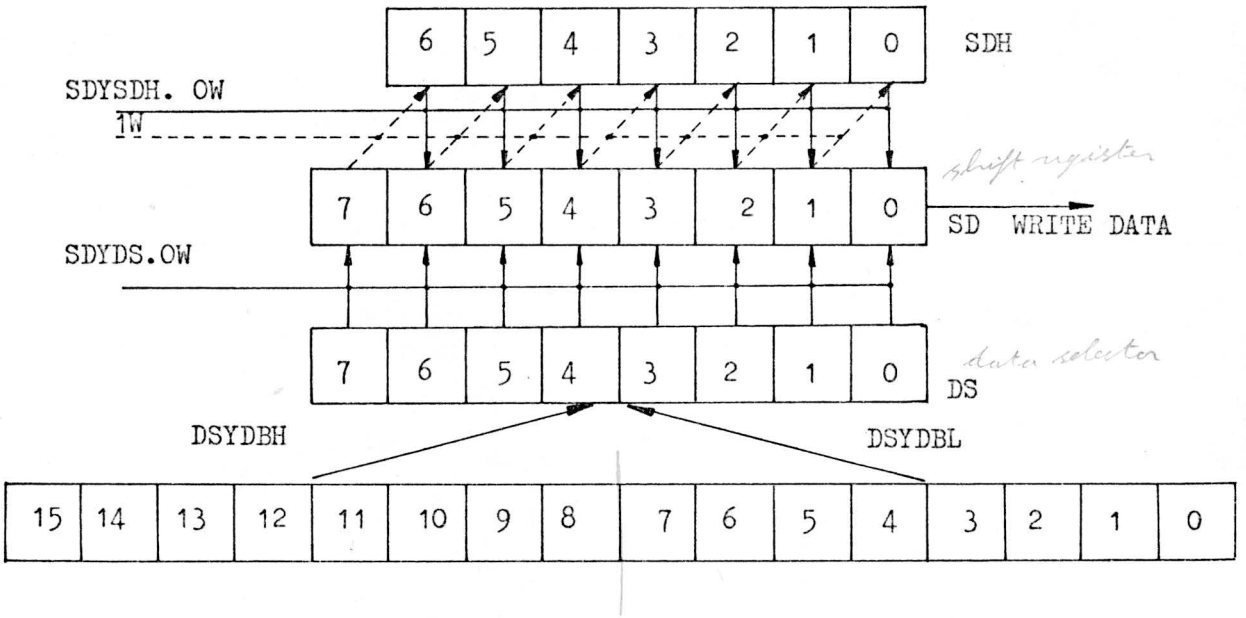
MP activates RTRC.

RTRC puts RTR in the cycle 0-1-2-3-0-1-etc., resulting in OR and 1R.

2. SERIALIZER-DESERIALIZER

2.1. WRITING

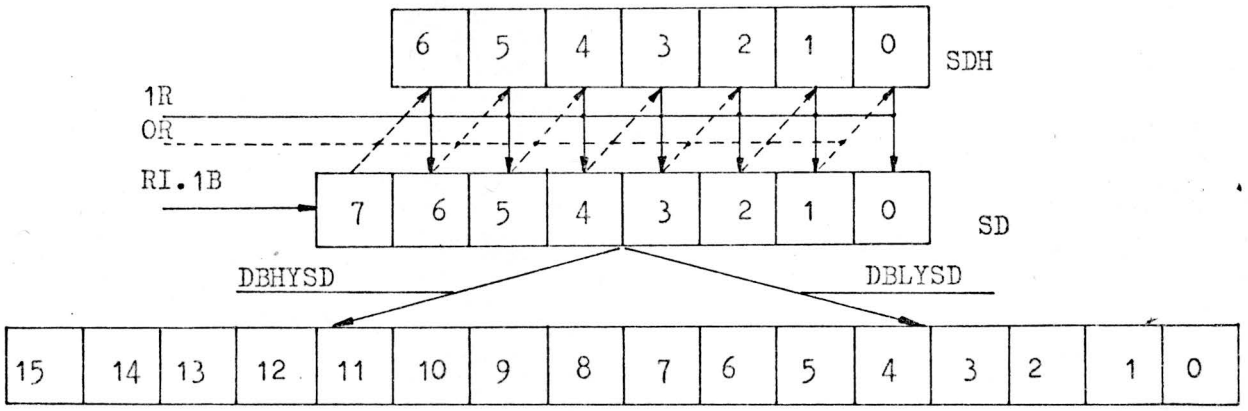
The shiftregister contains an 8-bits main- and a 7-bits secondary register.The data to be written is in a 16-bits DATA BUFFER (DB). Successively the contents of the upper and lower half of this data buffer is placed in the shiftregister (SD) via the DATA SELECTOR. The shifting takes place from most to least significant bit; the secondary register is read during 1W, the main register during OW. The least significant bit of the main register (SDo) controls the WTR as to the writing of "0"s or "1"s to the mono disk drive.



The macro-timings of the activating signals (DSYDBH,DSYDBL, SDYDS,SDYSDH) are derived from the Bitcounter and Wordcounter.

2.2. READING

During reading the READ INFORMATION arriving on SD7 is shifted from most to least significant bit. Reading of SD during 1R,and reading SDH during OR. The collected bytes are placed successively in the upper and lower part of the DATA BUFFER.



BITCOUNTER-WORDCOUNTER

The Bitcounter and wordcounter (BT, WT) are two 8-positions timing rings with fill up codes.

Codes :

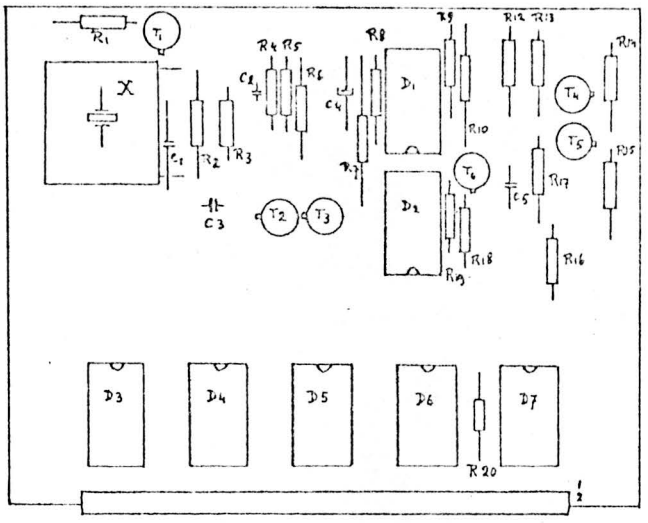
BT	0 1 2 3		WT	0 1 2 3	
0	0 0 0 0	1 RW. REDAT	0	0 0 0 0	BTS 34. 0 RW
1	0 0 0 1	0 RW	1	0 0 0 1	BTS 70. 0 RW
2	0 0 1 1	1 RW	2	0 0 1 1	BTS 34. 0 RW
3	0 1 1 1	0 RW	3	0 1 1 1	BTS 70. 0 RW
4	1 1 1 1	1 RW	4	1 1 1 1	BTS 34. 0 RW
5	1 1 1 0	0 RW	5	1 1 1 0	BTS 70. 0 RW
6	1 1 0 0	1 RW	6	1 1 0 0	BTS 34. 0 RW
7	1 0 0 0	0 RW	7	1 0 0 0	BTS 70. 0 RW

REDAT is the validation signal to start BT :

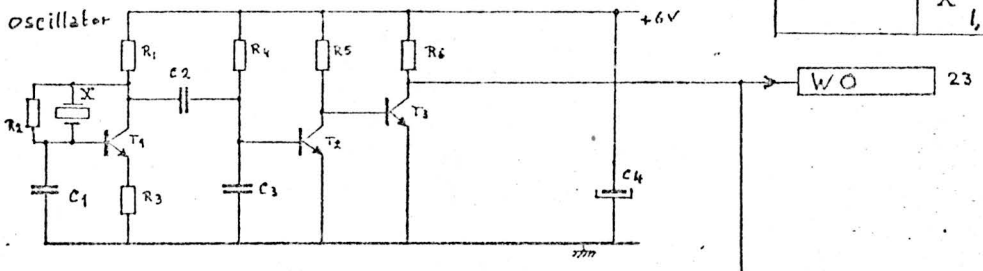
a. during WRITING the beginning of synchronizing pattern.

b. during READING the discovery of the synchronization pattern.

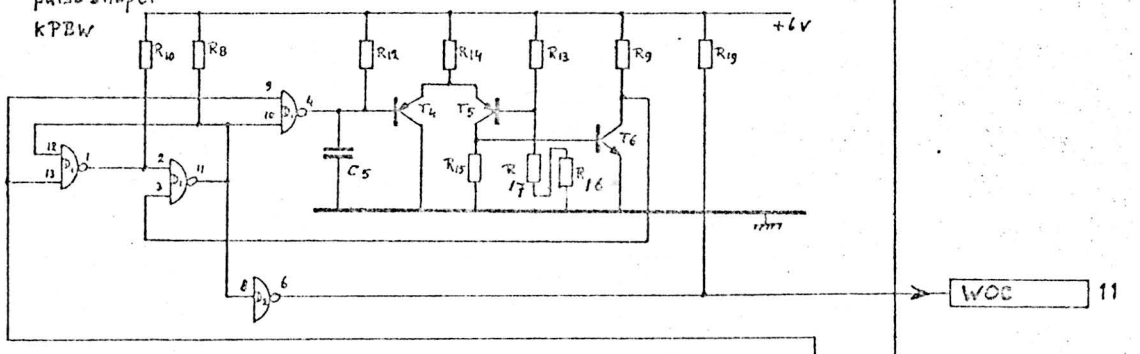
R1	1K	C1	100p
R2	12k	C2	1000 p
R3	47	C3	100 p
R4	2K15	C4	5µ
R5	1k21	C5	82 p
R6	270		
R7	178	D1	FCH 181
R8	560	D2	TAH 140
R9	1K	D3	FCH 131
R10	560	D4	FCH 131
		D5	FCH 191
R12	2k7	D6	FCH 101
R13	1K	D7	FCH 101
R14	2k2		
R15	1K	T1	BSX 20
R16	1k2	T2	BSX 20
R17	215	T3	BSX 20
R18	178	T4	BCY 70
R19	178	T5	BCY 70
R20	560	T6	BSX 20
		X	kristal 1,66700 Mc/s



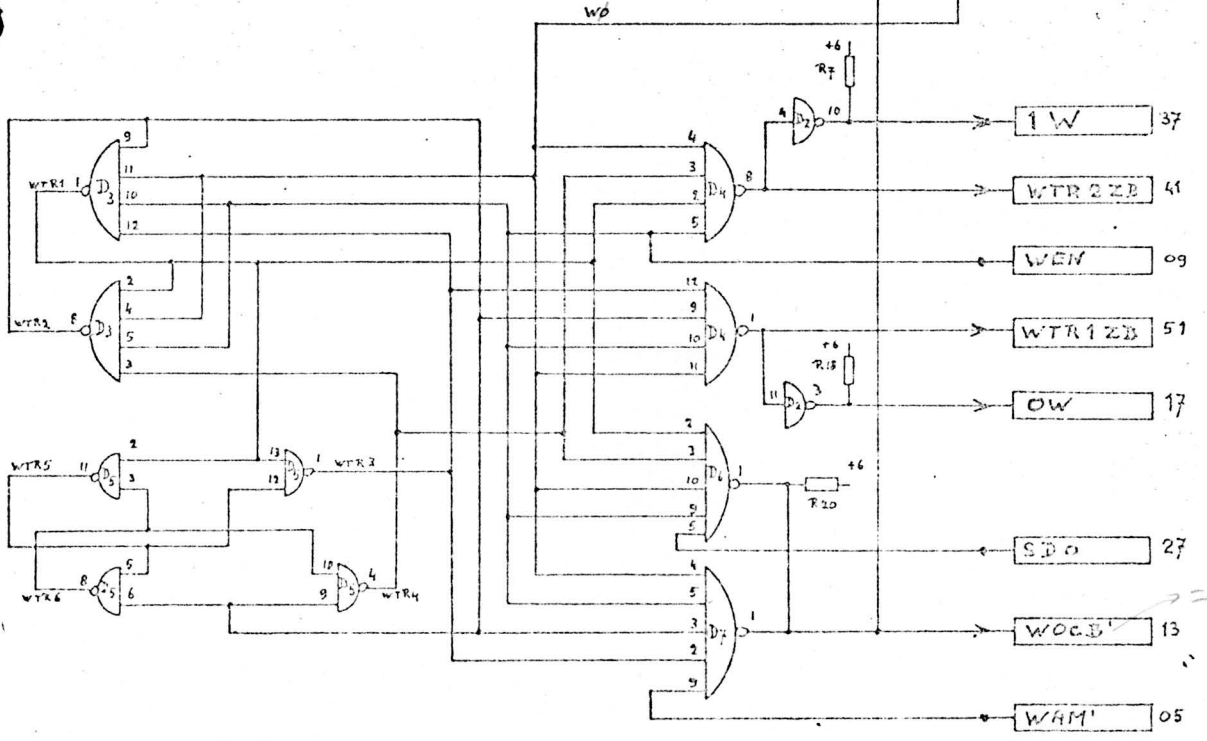
write oscillator



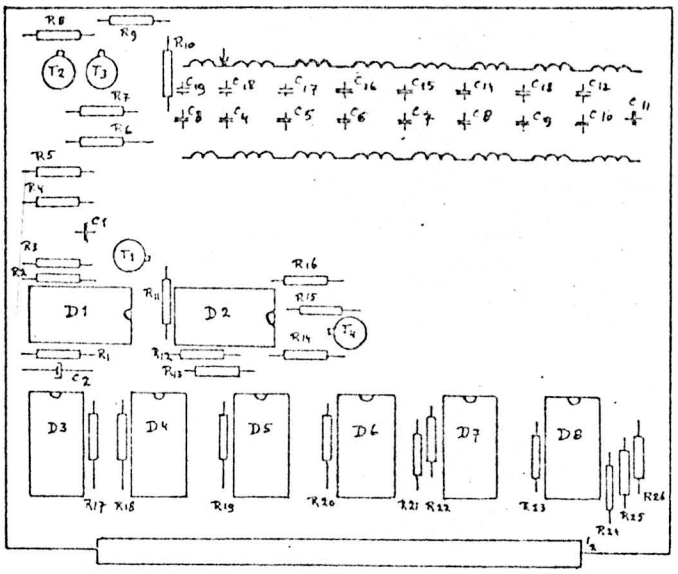
pulse shaper
KPBW



wo

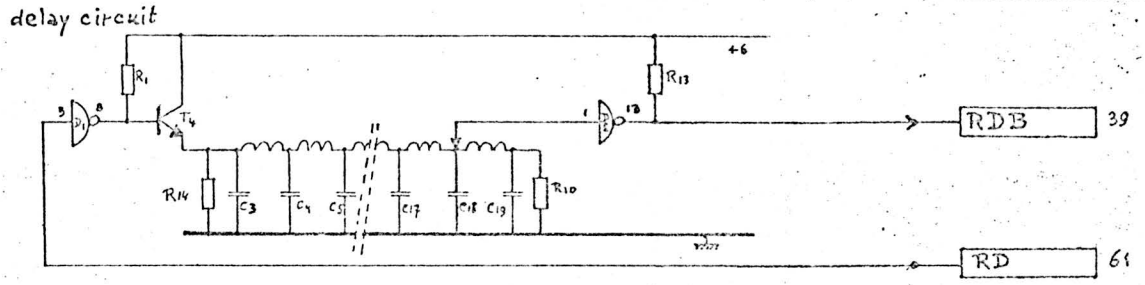


=WD unshaped

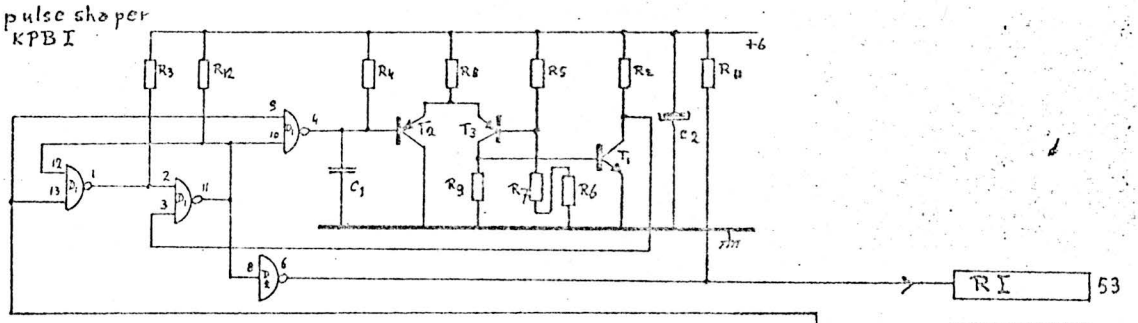


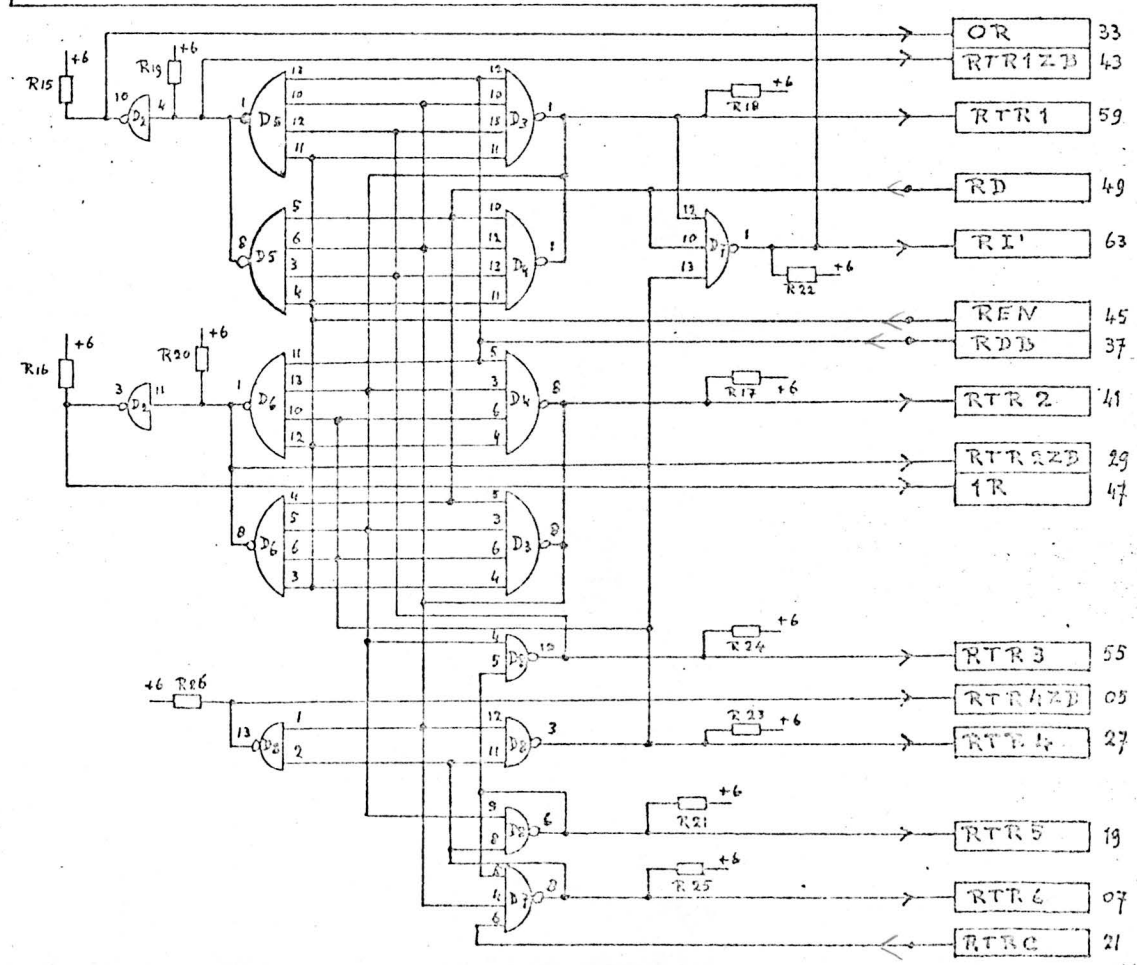
R1	562	T1	BSX20
R2	1K	T2	BCY70
R3	562	T3	BCY70
R4	2K61	T4	BSX20
R5	1K		
R6	1K	D1	FCH101
R7	330	D2	TAH140
R8	2.K15	D3	TAH120
R9	1K	D4	TAH120
R10	121	D5	TAH120
R11	178	D6	TAH120
R12	562	D7	TAH120
R13	178	D8	TAH140
R14	1K		
R15 t/m R26	178		
C1	82p		
C2	3.3µ		
C3 t/m C19	330p		

delay circuit



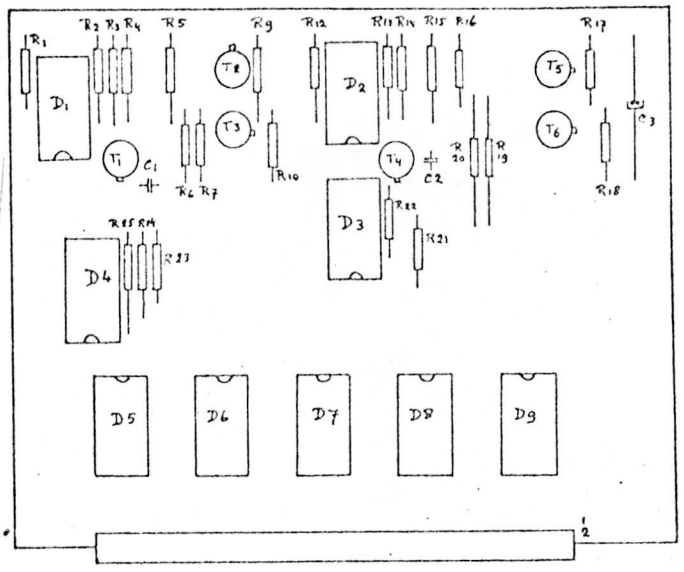
pulse shaper
KPB I



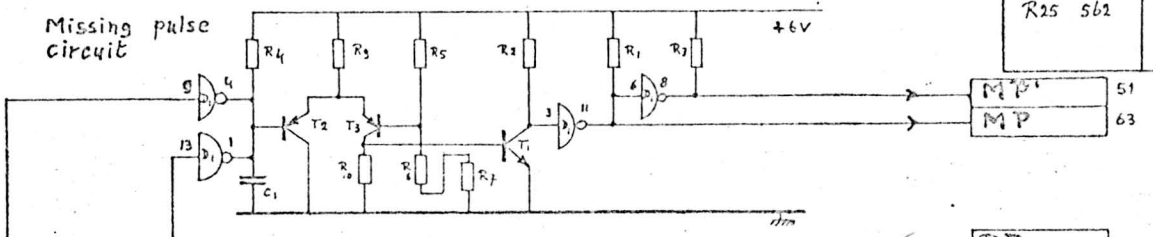


R1	562
R2	1K
R3	562
R4	2K64
R5	1K
R6	220
R7	27
R9	2K15
R10	1K
R12	562
R13	1K
R14	562
R15	2K64
R16	1K
R17	2K15
R18	1K
R19	1K
R20	390
R21	178
R22	178
R23	562
R24	562
R25	562

C1	1200 P
C2	82 P
C3	3,3 µ
D1	FCH 181
D2	FCH 181
D3	TAH 140
D4	FCH 181
D5	FCH 131
D6	FCH 171
D7	FCH 211
D8	FCH 181
D9	FCH 151
T1	BSX 20
T2	BCY 70
T3	BCY 70
T4	BSX 20
T5	BCY 70
T6	BCY 70



Missing pulse circuit



pulseshaper KPDR